Gavin Hsia

gavin.hsia5@gmail.com | 971-205-4368 | linkedin.com/in/gavinhsia | U.S Citizen

EDUCATION

Santa Clara University, BS in Electrical and Computer Engineering Expected June 2027

SKILLS

Languages: C, C++, Python, SystemVerilog, ARM Assembly
Design Tools: KiCad, Cadence Allegro, Cadence SKILL, Altium, Sigrity, LTspice, MATLAB
Lab Equipment: Vector Network Analyzer, Oscilloscope, Logic Analyzer, Soldering
Technologies: PCB Design, Signal Integrity, S-Parameters, Crosstalk Analysis, Clock Distribution, ITU-T G.703, Controlled Impedance, Microcontroller Bring-Up, I2C, SPI, Git, Linux, Jira, RTOS

EXPERIENCE

Networking R&D Hardware Design Intern, Hewlett Packard Enterprise June 2026 – Present

- Diagnosed an off-isolation failure in an ITU-T G.703 10 MHz timing circuit by measuring channel attenuation across the analog switch, current buffer, and comparator stages
- Traced the fault to an analog switch measuring 23 dB off-isolation at 10 MHz against a 40 dB datasheet specification, caused by excess channel coupling and crosstalk in the off state
- Characterized replacement switches on a vector network analyzer, scoring off-isolation, feedthrough capacitance, on-resistance, and bandwidth to qualify a compliant part
- Supported board-level integration of a central ASIC with the ASIC design team, defining pin-level interfaces, power and clocking requirements, and debugging bring-up issues
- Automated PCB net documentation with Cadence SKILL and Python, isolating the dominant etch layer per net and capturing a consistent-zoom image set that replaced manual review captures
- Audited controlled impedance nets in Cadence Allegro to locate trace neck-downs, ranking nets by minimum width across layers to flag geometry deviating from impedance targets

Wiring Integration Electrical Team, SCU Formula SAE Oct 2025 – Present

- Designed and validated vehicle-grade wiring harnesses for temperature and pressure sensing subsystems, maintaining signal integrity on runs to the driver display module
- Routed low-voltage power and control signals with a defined grounding strategy, sizing conductors and selecting connectors to survive vibration and dynamic load

Embedded Systems Engineering Intern, MOVD Jan 2025 – Apr 2026

- Designed and validated multiple KiCad PCB revisions for an ESP32 product, integrating power regulation, IO, and test points, and cut part count via rail consolidation
- Performed bring-up, functional validation, and failure isolation on prototype PCB assemblies using oscilloscopes and logic analyzers to resolve hardware defects before release

PROJECTS

10 MHz and 1PPS Reference Switching Circuit June 2026 – Present

- Selected a replacement analog switch for a 10 MHz and 1PPS reference distribution circuit, scoring candidates on off-isolation, crosstalk, feedthrough capacitance, and bandwidth
- Owned the redesign through bring-up, from schematic and isolation-conscious layout to fabrication, then validated insertion and return loss against G.703

Electrical System Integration Oct 2025 – Present

- Built low-voltage signal routing and power distribution for the vehicle temperature and pressure sensing subsystems
- Analyzed grounding strategy, fuse protection, and connector current ratings across the vehicle

Stratos Pro V3 Jan 2025 – Apr 2026

- Designed a custom ESP32 PCB with an integrated OLED display, improving system efficiency 15 percent through power rail and component selection changes

Real-Time Digital Filter Engine Mar 2026 – June 2026

- Implemented a difference-equation filter in C supporting FIR and IIR responses with circular buffers, validated on Cortex-M4 across Butterworth and Parks-McClellan designs